## REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

### Status of Claims

Claims 1 through 8 are pending in the application. Claims 1 through 8 have been rejected.

### CLAIM REJECTIONS

### 35 U.S.C. § 112 Rejections

In the Office Action, the Examiner had rejected claims 1 and 4 through 8, under 35 U.S.C. § 112, first paragraph. More specifically, the Examiner stated in the Office Action that he finds claims 1, and 4 through 8 to fail "to comply with the enablement requirement" because allegedly a limitation recited in claims 1 and 4, namely **"...storing in said NVM array the ECC and the block of bits from which the ECC was not derived..."**, is not sufficiently supported by the specification because the Examiner believes the limitation to only be mentioned as part of element 1000 in Fig.8.

Applicant respectfully disagrees with the Examiner's rejection. The allegedly unsupported limitation is inherent throughout the specification, and in Applicant's opinion was implemental by one of ordinary skill in the art of digital data storage at the time the present application was filed, assuming he or she had bothered reading the entire disclosure of the present application.

In support of Applicant's opinion and position, Applicant would kindly like to bring the Examiner's attention to the following sections from the original application:

- page 4, 1st paragraph, line no.5:

**"According to certain embodiments of the present invention, bits may be stored on the NVM array in the rearranged order, while in other embodiments of the present invention, bits may be stored on the NVM in their original order."**

- page 2, 2nd paragraph :

**"Since NVM based devices have a certain probability of bit read or write errors when being operated, controllers may include "Error Detection" and/or "Error Correction Coding" ("ECC") functionality. NVM chips or devices with built-in error-checking typically use a method known as parity to check for errors. The problem with parity is that it discovers errors but does nothing to correct them. Critical application may need a higher level of fault tolerance, and thus when storing data on an NVM array, controllers may produce an ECC associated with the data being stored and may store the ECC along with the original data. When reading the data from the array, the controller may use the data's associated ECC to recover data lost because of errors produced when either programming or reading the data."**

Since both the concept of storing a block of data, either in its original order or in a rearranged order, are well described throughout the specification, and since generating a ECC for a block of data (original block or rearranged block) was known at the time the present application was filed, it is Applicant's position that the allegedly unsupported limitation "...storing in said NVM array the ECC and the block of bits from which the ECC was not

derived" (i.e. the original block or the rearranged block), when read in the context of the rest of the claim, and in light of the specification as filed, is clear and fully supported. Accordingly, applicant respectfully requests that the Examiner withdraw his 112 rejections of claims 1 and 4 through 8.

**35 U.S.C. § 103 Rejections**

In the Office Action, the Examiner rejected claims 1 though 7 under 35 U.S.C. § 103(a), as being obvious and unpatentable over US PGPUB 2003/0135798 to Katayama et al (the "Katayama reference"). Applicants respectfully traverse the rejection of claims 1 through 7 under the Katayama reference, and thank the Examiner for at least implying that claim 8 is patentable over the Katayama reference.

Applicants respectfully traverse the Examiner's 103 rejections of claims 1 through 7 because a prima facie case of obviousness has not been established. As is well established in the patent law, to support an obviousness rejection requires a teaching or a suggestion by the relied upon prior art of all the elements of a claim (M.P.E.P. §2142). Since, however, the Katayama reference does not teach or suggest storing on an NVM both an ECC of a data block (i.e. ECC generated from original data block or some rearrangement of the original data block) and a different version/arrangement of the data block than the one from which the ECC was derived, a limitation present in independent claims 1 through 4, Applicants assert that independent claims 1 through 4 are not obvious over the Katayama reference and respectfully request that the Examiner withdraw his rejections of claims 1 through 4.

Since claims 5 through 7 depend from allowable claim 4, applicants consider these claims allowable by virtue of their dependence on an allowable base claim. Applicants therefore respectfully request that the Examiner withdraw his 103 rejections of claims 5 through 7.

In view of the foregoing remarks, the pending claims are believed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone

number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 50-3400.

Respectfully submitted,

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